5633031

B.Tech. DEGREE EXAMINATION,
NOVEMBER/DECEMBER 2016.

Third Semester

Computer Science and Engineering

DIGITAL SYSTEM DESIGN

(2013-2014 onwards)

Time : Three hours Maximum : 75 marks

PART A — (10 × 2 = 20 marks)

Answer ALL questions.

All questions carry equal marks.

1. Find the octal equivalent of decimal 200.

2. State De Morgan's theorem.

3. What is meant by decoder?

4. What is multiplexer?

5. What is ring counter?

6. What is JK flip-flop?

7. Distinguish between RAM and ROM.

8. What is meant by address decoding?

9. What is meant by gate-level modeling?

10. What is meant by dataflow modeling?

PART B — ($5 \times 11 = 55$ marks)

Answer ALL questions, choosing ONE from each Unit.

All questions carry equal marks.

UNIT I

11. Using the K-map method, obtain the minimal sum of product expression of the following function

$y = \Sigma(0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$.

Or

12. Find the minimal sum of products for the Boolean expression

$f(w, x, y, z) = \Sigma(1, 3, 4, 5, 9, 10, 11) + \Sigma\phi(6, 8)$.

Using the Quine-McClusky method. And also draw the logic circuit diagram.

UNIT II

13. Design a full subtractor using only NOR gates.

Or

14. Briefly discuss about parallel adders.

UNIT III

15. Explain about different types of Shift Registers in detail.

Or

16. Discuss about mealy and Moore models in detail.

UNIT IV

17. Briefly discuss about Programmable Array Logic (PAL) devices.

Or

18. Explain about different types of memories in detail.

UNIT V

19. Write notes on hierarchical Modeling concepts.

Or

20. Explain about 4-bit ripple carry counter in detail.
